Real-World Applications of Laser Direct Writing

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Abstract

Laser microchemical direct write deposition and etching methods have found an essential niche in debug and design for yield of wire-bonded and flip-chip integrated circuits. Future applications should develop in package-level system modification.

Introduction

In research dating back to the early 1980's laser and focused ion beam (FIB) direct write deposition and etching have been developed with an eye to a variety of microelectronic needs. The two methods referenced share much in the way of capabilities. Over time the two approaches have specialized and have been integrated into a powerful set of methods uniquely important to the microelectronics industry.

This paper will briefly summarize some of the established and emerging applications to more or less conventional circuit design debug; the elaboration of these methods to the particularly demanding testing and debug of packaged flip-chip parts, and the further evolution to package level debug. Surprisingly, the importance of this class of methods has been greatly intensified over the last several years. Leading microprocessor companies have begun to use FIB and laser direct writing methods to adjust designs to increase manufacturing yield and binning count at the factory as well as at the design center.

This paper will emphasize the practical applications of laser direct write methods and the integration of laser and FIB methods. The microchemical writing speed of the laser techniques are 2 to 6 orders of magnitude greater than they are for the ion beam analogs. Additionally, the electronic material quality of the laser deposited thin films are much higher, e.g. resistivity is typically 2 orders of magnitude lower than for the best focused ion beam deposited films. In the best cases the resolution of the laser techniques equal that of the dominant production technology for integrated circuits (ICs), which is optical lithography, but it cannot match the resolution of focused ion beams. As a result, users combine the virtues of both direct writing methods in actual practice. The diverse microchemical process technology used in laser direct writing is reviewed in Ref. 1.

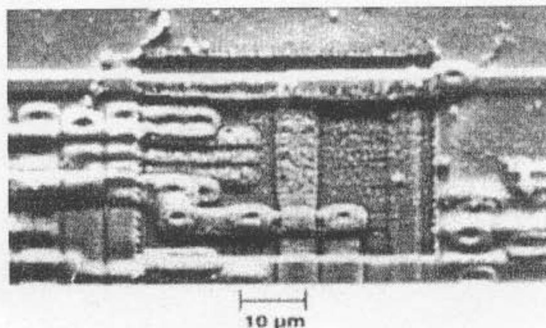

Figure 1: Conventional debug of a wire-bonded front-surface part requires penetration of a passivation layer. In this case a compound silicon nitride/silicon dioxide layer was removed by a laser technique. Laser methods for chip depassivation are generally chosen for their process speed.

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Design Modification of Conventional Wire-Bonded Circuits

The modification of conventionally bonded (circuit up) parts has been relatively straight forward as the electrical connection to individual transistors was possible through the passivation layer and the top of the part. Laser methods were chosen for long length discretionary interconnects over the passivation layer where the high conductivity and rate of laser deposited metal greatly exceeds FIB metal. Another application was removal of passivation, silicon dioxide, silicon nitride, polyimide, etc., where the rate of laser depassivation greatly exceeds the FIB (e.g., see Fig. 1). Two developments have complicated these applications; (1) the low accessibility of transistor connections due to multi-layer metallization, which now often covers >90% of the available surface, and (2) a strong trend toward nearly exclusive use of flip-chip circuits for high end systems. Both developments are driving design debug from the backside of the chip through the full thickness of the silicon wafer.

Flip-Chip Repair Process Flow

The debug/repair of flip chip parts imposes one new problem, the removal of the bulk silicon substrate in order to access the active device. Once this step is accomplished, probing and repair can proceed in analogy with more conventional front surface rework; examples being the use of a focused ion beam (FIB) to edit a circuit, or make probe points and a 3-beam prober for testing the circuit [3]. In fact access of active areas from the backside is often simpler and more easily interpreted than access through multi-level metallization. On integrated circuits in which the metallization completely covers the active device, diagnostic techniques such as photoemission must be completed from the backside.

Figure 2 depicts a flip-chip repair process flow. The first step is to globally thin the flipped part to a thickness that still maintains adequate mechanical strength and thermal dissipation capability. Typically a flip-chip may be globally thinned to 200μm using mechanical polishing without risking stress-induced fracture. This thickness is also sufficient for infrared through wafer viewing and global photoemission surveys.

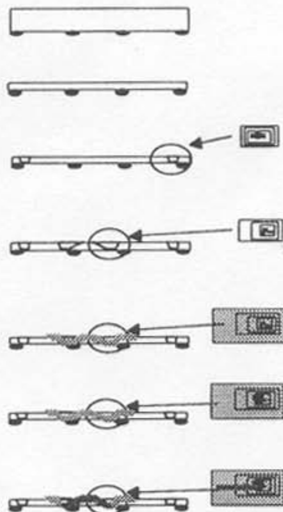


Figure 2: **Flip-Chip Repair Process Flow**

The second step is to reference front side fiducials in order to navigate to debug/repair sites. If accurate through wafer viewing is not available, trenches may be efficiently etched to the front surface. The laser microchemical process can etch completely to the field oxide, since oxide is an etch-stop layer, or leave a thin silicon layer to be processed by other tools. Other tools (e.g. a FIB) can locate the fiducials either optically or by etching through the remaining field oxide until the metal fiducial is exposed. Three fiducial trenches (200μm x 200μm x 200μm) can be laser processed in about thirty minutes.

The third step is to access circuit debug/repair sites by etching laser microchemical trenches over the regions of interest. Placement of these trenches may be aided by the use of computer aided navigation (CAV) e.g. Knight Navigation to correspond circuit to layout and navigate the laser microchemical etcher. Trenches need not be placed with extreme accuracy since they may be efficiently etched to hundreds of micrometers across; the trenches must, however, be flat, uniform, and stop close to the active device.

The fourth step is to deposit a dielectric isolation layer on the bottom and sidewalls of the trench. This can be accomplished globally as a separate step (typically time consuming), or locally using laser deposited oxide.

The fifth step is to make local repairs at the base of the isolated trenches. These repairs can be similar to those performed on the front side of the chip due to the proximity of the trench base to the active device. Typically a focused ion beam is used to create a high aspect ratio via to the node to be tested or rewired. For interconnects longer than a few tens of micrometers, laser deposition can be used to make interconnects with about 3μohm-cm conductivity.

The final step, if necessary, is to interconnect repairs between trenches. In this case a laser deposited interconnect is run up the sidewall of one trench over the top of the substrate and back down into another trench. Figure 3 shows a scanning electron micrograph of a typical laser etched trench.

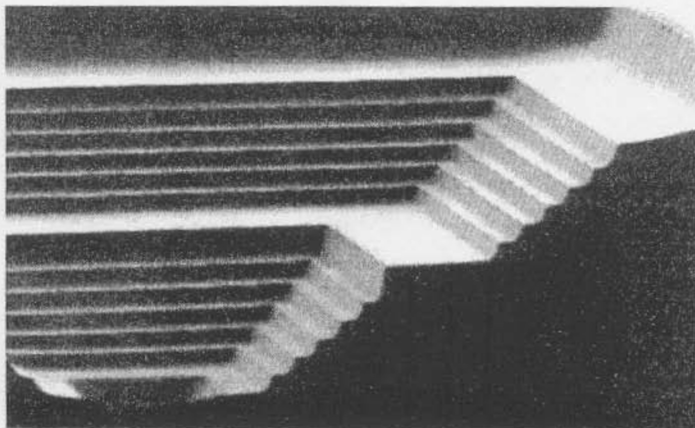


Figure 3: A silicon trench etched using chlorine-assisted chemistry from the backside of a flip-chip integrated circuit. The terracing is more pronounced than typically necessary for the application. The above figure shows an excellent example of the process cleanliness and control possible with the laser method. (the typical depth is ten microns per small terrace in the scanning electron micrograph).

OBIC Endpointing Method

Laser microchemical processing enables efficient access to flip-chip devices for debug and repair. To be effective, the etched trenches must be flat, uniform, and stop close to the active device. The closer the base of the trench is to the active device the easier it will be to implement an edit. The required aspect ratio of a via made with a focused ion beam can double if the via must first be milled through tens of micrometers of silicon before accessing the diffusion regions.

The laser etch process is not typically the limiting factor in producing trenches close to the active device since the microchemical zone, the region melted by the laser and reacted with a gaseous ambient, is highly confined. Instead, knowing when to stop determines how close the base of the trench will be. If the initial surface is uniform and the thickness of the substrate is well known, the trench can be etched using dead reckoning, relying on the repeatability of the etch process to approach the active region. Typical long-term repeatability of trenches up to 200μm deep in homogeneous silicon is less than 2μm.

In general, the back surface of a flip-chip is not uniform after mechanical polishing to 200μm or less and the remaining thickness is not well known. An infrared confocal microscope can be used to measure the remaining thickness of silicon if the dielectric constant of the substrate is precisely known.

To eliminate the uncertainties of the substrate thickness and uniformity, the active device may be used as a reference. Laser microchemical etching of the backside of the flip-chip induces a current which may be measured between Vcc and GND. Figure 4 depicts schematically the fixture and electronics used to measure the induced current.

The fixture consists of a zero insertion force Socket 7 mounted on an aluminum stand inside the etch process chamber. Connections to the device are made via a vacuum feedthrough. Solder surfaces are coated so as not to react with the process gas and contaminate the chamber. A simple transimpedance amplifier is used to convert the current to a voltage that can be read by a control computer using an analog to digital converter.

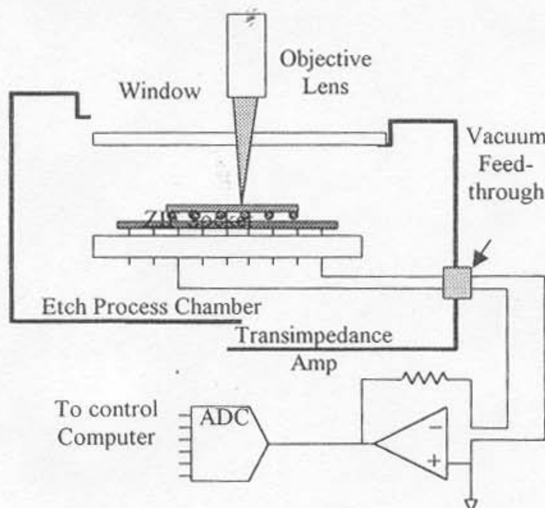


Figure 4: OBIC Endpoint Fixture and Electronics

A trench is etched by scanning an argon-ion laser (multi-line with primary wavelengths of 488nm, 514nm) across the silicon removing one layer at a time. Initially etching is done at 5 to 7µm per scan and then slowed to less than a micrometer per scan when approaching the active region. The induced current is measured during each scan line near the center of the trench. Figure 5 shows the current as a function of scans. Since the silicon strongly absorbs at visible wavelengths, the signal is sensitive to submicrometer thickness changes. By calibrating the signal to remaining thickness and using a threshold to complete the scan and then stop, the trench may be accurately etched to a known thickness from the active device.

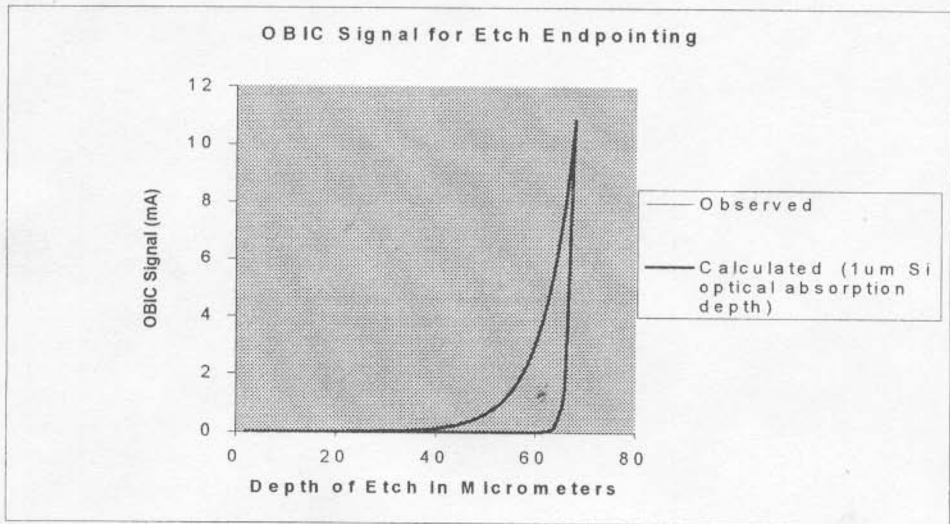
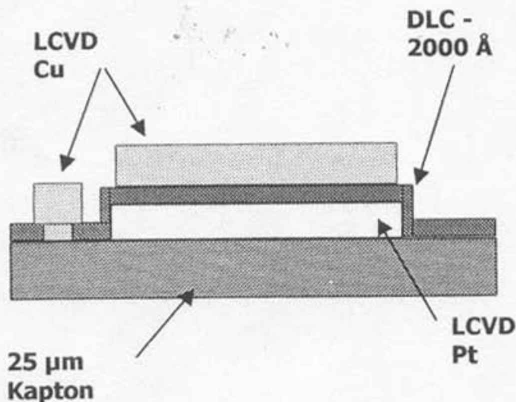


Figure 5: Measured OBIC current as a function of etch depth for a typical flip-chip part.

Package Level System Debug

As microprocessors migrate to multiple chip modules and as portable communication devices gather complexity and increasing integration, it is clear that direct writing methods will be required to debug systems at the package level. Methods for circuit adjustment on ceramic, laminate and flex-circuit packaging will be necessary. Many of the laser deposition chemistries developed for chip level will be equally applicable at package level. In addition there may be an opportunity of laser direct write techniques that will fabricate precision passive elements such as resistors, capacitors and inductors. These package level fabrication methods will need to be coupled closely to test apparatus to achieve highly precise passive tolerance. An example of a demonstration of this application is shown in Figure 6. The process challenge for capacitors and inductors is to achieve consistent, high quality dielectric deposition with a process step that remains compatible with a direct write electrode-patterning method.



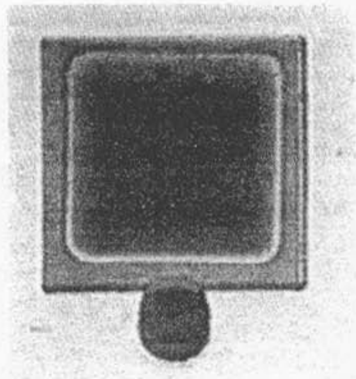


Figure 6. Demonstration of a capacitor on a free standing Kapton film, with laser deposited top (copper) and bottom (platinum) electrodes and plasma deposited dielectric (diamond like carbon). This device is approximately 500 microns square, with a measured value of 58 pF, low leakage and a Q of 30 at 1 MHz frequency. (Photo courtesy of Donald Foust, General Electric Corporate Research and Development).

Conclusion

We have reviewed the application of laser microchemical direct writing techniques as they are currently applied in silicon circuit debug and yield enhancement. These methods are now securely placed as part of the essential tool set for cost-effective manufacturing of microprocessors and other complicated silicon systems. Future technology trends will probably push applications of similar laser methods into use at the package level. These methods may involve laser fabrication of full discrete passive elements (resistors, capacitors, and inductors) as well as interconnect.

References

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