high density optoelectronic circuits which takes full advantage of commercial VLSI GaAs MESFETs.

*Annette C. Grot and Demetri Psaltisis are with the California Institute of Technology, Room 116-81, Pasadena, CA 91125 Tel. (818) 356-3893.

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VIA-4 Characterization and High-Speed Digital Application of GaAs MESFET's on Substrates—S. Onozawa, N. Yamamoto, T. Kimura, Y. Sano, and M. Akiyama, Oki Electric Industry Co., Ltd., 550-5 Higashiasakawa-cho, Hachioji, Tokyo 193, Japan Tel. 0426-63-1111.

Crystallinity of GaAs epilayers on Si has shown a great improvement owing to the 2-step growth technique [1] and many devices fabricated on the GaAs/Si substrates have been reported. However, there still exist several problems due to the nature of the substrate for submicron devices. The most serious is a strong residual stress of about 10^9 dyn/cm^2 between GaAs and Si, which induces piezoelectric charges and causes a large shift of threshold voltage of a few hundred mV for submicron gate GaAs MESFET's. We have solved this problem by introducing p-layer (C^+: 140 keV) burried under the n-type channel (Si^+: 20 keV) in the n^+ self-alignment technique with refractory W-Al gate [2]. The device fabricated with a 0.3 μm-gate showed good saturation characteristics and high transconductance of 498 mS/mm, of which value is only 4% smaller than that of a control device on a GaAs substrate. These results indicates that the crystallinity of the GaAs epilayer such as the electron mobility is good enough for the high speed device application.

Then, uniformity becomes the next requirement for the large scale integration. We evaluated, for the first time, the microscopic uniformity of the device on GaAs/Si using 60 μm $\times$ 60 μm-pitch FET arrays, and found that it is remarkably improved by introducing the p-layer. The standard deviation of the threshold voltage for 900 FET's (with p-layer) within an area of 3.6 $\times$ 0.9 mm^2 was as small as 20.3 mV, which is about a half of that for the control device (without p-layer).

Finally, to evaluate the dynamic characteristics, we fabricated a direct-coupled FET logic (DCFL) ring oscillator using the 0.3 μm-gate MESFET on the GaAs/Si substrate. As a result, the propagation delay was as small as 19.9 ps/gate at a supply voltage of 2 V. We also fabricated an 1/2 frequency divider. The circuit, designed by the memory-cell type flip-flop (MCFF) [3], showed a stable operation up to 10 GHz, which is the highest speed ever reported for GaAs/Si devices.

In summary, we optimized the device structure to suppress the short channel effect due to the residual stress in GaAs/Si substrates and improved the microscopic uniformity, then successfully fabricated a high speed digital circuit. From the results obtained we have proved that the technology of GaAs/Si can provide large and high-quality substrates for high speed large scale integration.

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VIA-5 Demonstration of Monolithic Co-Fabrication of $Y_1Ba_2Cu_3O_{7-\delta}$ and CMOS Devices on the Same Sapphire Substrate—P. R. de la Houssaye, M. J. Burns,* W. J. Ruby,* S. D. Russell, S. R. Clayton, G. A. Garcia, L. P. Lee,* NCCOSC RDTE DIV (NRaD) 553, 49375 Ashburn Rd., Room 2, San Diego, CA 92152-7633.

We report the first fabrication of active semiconductor and high temperature superconducting (HTS) devices on the same substrate. Complementary Metal-Oxide-Semiconductor (CMOS) transistors were fabricated on the same sapphire substrate as either YBCO flux-flow transistors (FFT's) or YBCO superconducting quantum interference devices (SQUID's). All devices functioned as expected at 77 K without degradation, demonstrating that a compatible process has been found to monolithically integrate adjacent CMOS and HTS devices.

In the seven years since the discovery of high-temperature superconductivity, the field of superconductive electronics has undergone explosive development. Due to difficulties in growing films directly on silicon, copper and oxygen contamination of the silicon layers during growth, and the high temperature environments seen in HTS growth, it has not been fully integrated with semiconductor based technology. Research has been focused on the use of superconducting interconnects between integrated circuits, which could lower chip power dissipation, reduce necessary interconnect width and pitch, and reduce dispersive loss. Several attempts have been made to fabricate HTS circuits or devices directly on Si or other semiconductor surfaces [1], [2]; these layers were of low quality and were stress limited, and no devices were fabricated in the layers.

CMOS thin-film silicon on sapphire (SOS) devices utilizing improved silicon films have achieved performance equal to or better than bulk CMOS devices [3]. For low temperature, low power operation, CMOS SOS has a number of advantages over other silicon technologies [4]. Additionally, one of the best substrates for growth of YBCO layers for superconducting devices is sapphire.

Fabrication of the thin-film SOS CMOS on sapphire was performed first. Further details relating to the CMOS pro-

cessing in SOS can be found in Offord [3]. Areas that were to later have HTS devices were initially protected from various silicon processing steps such as high energy ion implants by initially not removing the silicon layer from the area. In CMOS circuit fabrication, a layer of aluminum is typically used as the interconnect layer between devices. Aluminum, however, cannot withstand the processing temperatures incumbent in superconducting device fabrication. For short distances, this layer was replaced by a second polycide ($TiSi_2$) layer. After CMOS processing was complete, the silicon protective coating was removed in the HTS area and a 200 nm layer of Si_3N_4 was deposited and patterned over the CMOS devices as a final passivating layer against the oxygen plasma and copper environments seen during the YBCO growth.

YBCO devices were then fabricated on the bare sapphire adjacent to the test CMOS devices, aligned lithographically. Pulsed laser deposition (PLD) techniques were used [5] in conjunction with a series of buffer layers [6]. For the production of grain-boundary SQUID's, these buffer layers include final MgO and CeO layers used to produce a 45° in-plane rotation where desired. YBCO deposited over the Si_3N_4 regions was not superconducting. An amorphous Al_2O_3 layer was used as a passivation of the YBCO devices. Openings for electrical contact to both the YBCO devices and the CMOS can be made using photolithography and RIE or ion milling and a final layer of metal can easily be patterned for a final interconnection layer.

Both bi-epitaxial and step edge SQUID's were made with modulation voltages at 77 K as large as 40 $\mu V/F_0$. *I–V* curves from both p- and n-MOS devices were measured and compared with devices which did not receive HTS processing. No significant difference was seen.

This demonstration opens up numerous other possibilities to explore the combination of these two well developed technologies. Circuits and devices that exploit the advantages of both HTS materials and SOS CMOS in order to mitigate the deficiencies of the other can be integrated together. For example, ultra-sensitive SQUIDs, bolometers, and ultra-high speed Flux-Flow Transistors and Josephson Junction based circuits (functioning at speeds of 100 GHz or more) can be combined with CMOS memories, latches, low noise amplifiers, silicon based sensors, and driving electronics.

*M. J. Burns, W. J. Ruby, and L. P. Lee are with Conductu, Inc., 969 W. Maude Ave., Suunyval, CA 94086.

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VIA-6 High Temperature Superconductor Subharmonically Pumped Digital Phase Modulator/Demodulator—Lawrence Drabeck, Paul Polakos, Megan O'Malley, Martin V. Schneider, Ralph Trambarulo, and Paul Mankiewich,* AT&T Bell Laboratories, Holmdel, NJ 07733 Tel. (908) 888-7139 Fax (908) 888-7074.

We have incorporated high temperature superconducting technology along with conventional semiconducting elements into the design of a subharmonically-pumped digital phase modulator and demodulator capable of Gb/s transmission rates. The appropriate bandpass filters, stopband filters, and matching networks are fabricated from post annealed double sided $YBa_2Cu_3O_7$ films on 10 mil $LaAlO_3$. Typically these films have $T_c > 90$ K, $J_c > 2 \times 10^6$ A/cm^2 at 77 K and surface resistance at 10 GHz and 77 K of ~ 0.6 mOhms/sq.

The use of superconducting microstrip filters and matching elements with conventional nonlinear devices provides significant performance improvements. These improvements include higher bit rates, lower intersymbol interference, and lower conversion loss than for conventional circuits. Also, improved bit error rates, reduced device size due to higher dielectric constant substrate, and the potential for incorporating stable superconducting resonator pump sources on the same substrate are possible. In addition, as the technology matures, it is foreseeable that the conventional non-linear mixing elements will be replaced by superconducting bridges or junctions.

The device uses the mixing properties of nonlinear elements with antisymmetric *I–V* characteristics to generate the carrier and modulate its phase. The circuit consists of tandem rails operating in quadrature and permits modulation as well as recovery of data at greater than 1 Gb/s per rail. The modulator/demodulator pair is subharmonically pumped by the local oscillator (LO) at 9.5 GHz. The local oscillator is split and phase delayed by $\pi/4$ in one rail to give the correct orthogonality between rails. The local oscillator and the in-phase (I) and quadrature (Q) bit stream rails are isolated by bandpass and stopband filters. The circuit operates in either direction (acting either as a modulator or demodulator). Operating as a modulator, the local oscillator is upconverted and multiplied by the digital bit stream via antiparallel GaAs Schottky diode pairs to produce a phase encoded RF carrier at 19 GHz. Operating as a demodulator, the phase encoded RF signal is split and mixed with the second harmonic of the LO to produce two isolated bit streams.

A pair of modulator/demodulator circuits were hooked up in a loop-back configuration so that circuit performance could be studied. During testing, the devices were cooled to 75 K in a closed cycle refrigerator. A common local oscillator was used to pump both the modulator and demodulator. A pseudorandom bit stream was fed into the modulator and the phase-modulated signal was looped back to the demodulator to recover the original bit stream. Bit streams up to 1.244 Gb/s per rail were recovered with bit error rates less than 10^{-11}.