Demonstration of $Y_1Ba_2Cu_3O_{7-\delta}$ and complementary metal-oxide-semiconductor device fabrication on the same sapphire substrate

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We report the first fabrication of active semiconductor and high-temperature superconducting devices on the same substrate. Test structures of complementary metal-oxide-semiconductor transistors were fabricated on the same sapphire substrate as test structures of $Y_1Ba_2Cu_3O_{7-\delta}$ flux-flow transistors, and separately, $Y_1Ba_2Cu_3O_{7-\delta}$ superconducting quantum interference devices utilizing both biepitaxial and step-edge Josephson junctions. Both semiconductor and superconductor devices were operated at 77 K. The cofabrication of devices using these disparate yet complementary electronic technologies on the same substrate opens the door for the fabrication of true semiconductive/superconductive hybrid integrated circuits capable of exploiting the best features of each of these technologies.

Operation of semiconductor devices at liquid nitrogen temperatures continues to be investigated as computer manufacturers try to increase the speed of their devices.[1] A factor of 2 or more increase in speed for complementary metal-oxide-semiconductor (CMOS) devices can be obtained, a significant advantage for high performance computer systems.

While superconducting devices have much higher theoretical limits for speed than semiconductor devices, there are certain functions which they cannot perform well, particularly in the case of high temperature superconductor (HTS) devices. Superconductor device signal levels are typically millivolts, making such circuits difficult to interface to conventional electronics. Latches for readouts are difficult to design and implement in HTS because HTS junctions are not hysteretic. Semiconductor devices can easily be used to form latches and the level-shifting interface circuits digital superconducting circuits require.

The combination of both superconductor and semiconductor devices on the same chip operated at cryogenic temperatures could exploit the unique advantages of each technology; the symbiosis could lead to performance unattainable by either alone. Superconductor–semiconductor hybrid systems have been of great interest in recent years. Much of the work has centered on superconducting multichip modules in which bare semiconductor die are wired together using passive superconducting traces.[2] While the possible increases in electronic system performance and functional density using superconducting multichip modules is impressive, the full power of such hybrid systems may require the true integration of the full features of the two technologies on the same substrate.

In this letter we report for the first time the fabrication of $Y_1Ba_2Cu_3O_{7-\delta}$ (YBCO) test devices and Si CMOS test devices on the same chip. The YBCO devices and interconnects and CMOS devices can be connected with thin layers of Ag or Au, but this study was concerned with cofabrication and so the YBCO and CMOS test devices were not interconnected.

The cofabrication of YBCO and CMOS devices requires a substrate which allows the epitaxial growth of YBCO and Si is chemically stable at elevated temperatures in high O_2 environments, and does not allow the diffusion of Cu, Y, or Ba. It also requires the development of a method to protect each technology from the processing steps of the other. YBCO growth on buffered silicon (Si) and gallium arsenide (GaAs) has been demonstrated.[3,4] However, Si and GaAs wafers are not likely to be suitable candidates due to the high mobility of Cu and its behavior as a deep trap. In addition, the large mismatch in thermal coefficients of expansion between the semiconductors and YBCO precludes growth of thick YBCO films.[3] Copper is an interstitial-substitutional diffuser[5] in Si and GaAs, which at typical YBCO growth temperatures ($\sim$750 °C) can diffuse millimeters in an hour.[6] Thus, a substrate which does not allow diffusion of Cu, Ba, or Y but allows the epitaxial growth of YBCO and Si would be most desirable. Two such substrates have been identified—sapphire (Al_2O_3) and yttria stabilized zirconia (YSZ). Due to the existence of a highly developed silicon-on-sapphire (SOS) CMOS technology,[7] sapphire was the substrate choice for this study. Also SOS has been demonstrated to operate satisfactorily at low temperatures.[8] Use of SOS wafers limits the required diffusion barriers to top coverage of the silicon islands, so the total area of the diffusion barrier which must be defect-free is quite small. A pinhole in the diffusion barrier will result in copper contamination of only that island, and hence render a single subcomponent on one die unusable rather than the whole wafer.

The fabrication process is performed in four stages: (1) fabrication and patterning of the CMOS devices on SOS wafers, (2) encapsulation of the CMOS devices under a copper diffusion barrier, (3) growth and patterning of the YBCO structures, and (4) opening of contacts through

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the diffusion barrier to permit electrical access to the CMOS contacts. The processing order is dictated by the phase stability of the YBCO. The Si processing involves growth, diffusions, and annealing at temperatures up to 1000 °C. YBCO is grown at ~750 °C and irreversibly decomposes into various copper, yttria, and barium oxides above ~950 °C. Processing temperature for the YBCO and the associated buffer layers never exceeds 800 °C, at which the CMOS structures are quite stable.

Fabrication of the CMOS devices commenced with the formation of high quality single-crystal silicon films on 100 mm diam sapphire substrates using a regrowth process described elsewhere.[9] Thinning by oxidation and stripping reduced the silicon film thickness to a 100 nm thick device quality film. *P*-channel devices received a Boron *p*-well implant of $2.5\times10^{12}/cm^2$ at an energy of 35 keV through a 70 nm oxide. Gate oxide thickness for the FETs was approximately 23 nm. Further details relating to the CMOS processing in SOS can be found in Offord.[13] Areas that were to later have HTS devices were initially protected from various silicon processing steps such as ion implantation by initially not removing the silicon layer from the area.

The major modification to standard SOS FET fabrication techniques necessary for it to be compatible with HTS processing is the elimination of aluminum or other metals which decompose at the HTS processing temperatures. Though it would be possible to form all interconnects in the CMOS circuit after the opening of contacts through the diffusion barrier, it is desirable to have a level specific to the CMOS to allow for intermediate testing and higher density interconnects. For this purpose we used a polycide ($TiSi_2$) interconnect layer. After CMOS processing was complete, the silicon protective coating was removed in the HTS area using a combination of reactive ion etching (RIE) and wet chemical etching.

Finally, in preparation for HTS circuit fabrication, a 200 nm film of silicon nitride (Si_3N_4) was deposited using chemical vapor deposition (CVD). This layer was then patterned and etched off those regions to be utilized for HTS fabrication by RIE using a thin, CVD deposited, SiO_2 mask. Si_3N_4 has been demonstrated as a diffusion barrier for copper[10] and is known to also be a barrier for oxygen, which is necessary because of the oxygen plasma and copper environments seen during the YBCO growth. At this point, the wafer was sawed into pieces, each with areas of bare sapphire and passivated CMOS devices to allow for easier handling in the following HTS steps.

For the production of grain-boundary SQUIDs, pulsed laser deposition (PLD) techniques were used which have been described elsewhere.[11] The growth of the YBCO was preceded by PLD growth of a series of buffer layers composed of CeO, $Pr_1Ba_2Cu_3O_{7-\delta}$ (PBCO), $SrTiO_3$, MgO, and CeO. Deposition of these buffer layers has been described elsewhere.[3] The MgO layer was used to produce an in-plane 45° rotation of the CeO, which the YBCO follows when later epitaxially deposited. To define the grain boundary junctions, these buffer layers were patterned using standard photolithography and the top CeO and MgO layers were ion milled away in places where the 45° in plane rotation was *not* wanted. Another 10 nm of CeO was deposited by PLD followed by 300 nm of YBCO. It should be noted that while the entire substrate was covered by these buffer layers and YBCO, epitaxial growth occurred only on the bare sapphire regions. The amorphous layers which form over the Si_3N_4 and SiO_2 covered CMOS were not superconducting. The YBCO was then patterned into the appropriate SQUID geometry using standard photolithography and ion milling. An amorphous Al_2O_3 layer was then deposited over the substrate by PLD. Openings for electrical contacts to the YBCO SQUIDs were defined by standard photolithography and opened by ion milling. The ion sputtered contacts and modulation coils consisting of 250 nm Ag followed by 250 nm of Au were then deposited and patterned using standard liftoff techniques.

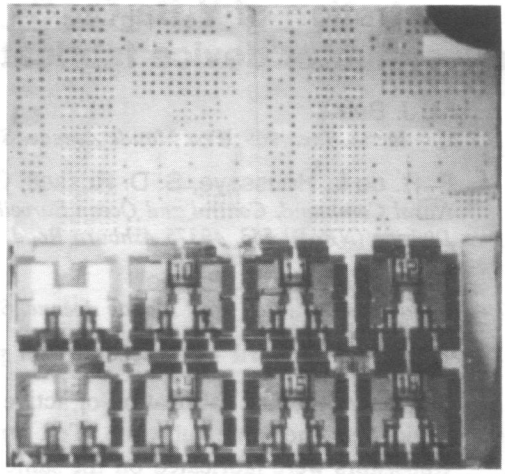

FIG. 1. A 1 cm×1 cm square sapphire substrate containing functional CMOS transistors and YBCO biepitaxial SQUIDs. Top half contains the CMOS with the YBCO devices on the bottom.

For the production of superconducting flux-flow transistors, step edge Josephson junction SQUIDs, simple wires and other nongrain boundary structures, the growth of the YBCO was preceded by PLD growth of 20 nm of CeO. These structures were then patterned using photolithography, ion etching, and wet etching.

The amorphous CeO, PBCO, STO, MgO, CeO, YBCO, and Al_2O_3 which formed over the Si_3N_4/SiO_2 covered CMOS was removed by ion milling. Contacts to the CMOS were opened through the diffusion layer by ion milling, reactive ion etching, etching in pure phosphoric acid at a temperature between 155 and 160 °C, or a combination of all three.

In Fig. 1 we show a 1 cm×1 cm sapphire chip, half covered by CMOS test transistors and half-covered with biepitaxial SQUIDs. In Fig. 2(a) we show the ~0.3 μV modulation of one such biepitaxial SQUID at 77 K and in Fig. 2(b) we show a step edge SQUID ~40 μV modulation at 77 K. In Fig. 3 we show the *I-V* curve of a superconducting flux-flow transistor at various control line currents at 77 K.

In Fig. 4(a), we show the *I-V* curves of a *n*MOS transistor measured at 300 K with a gate length of 3 μm and a

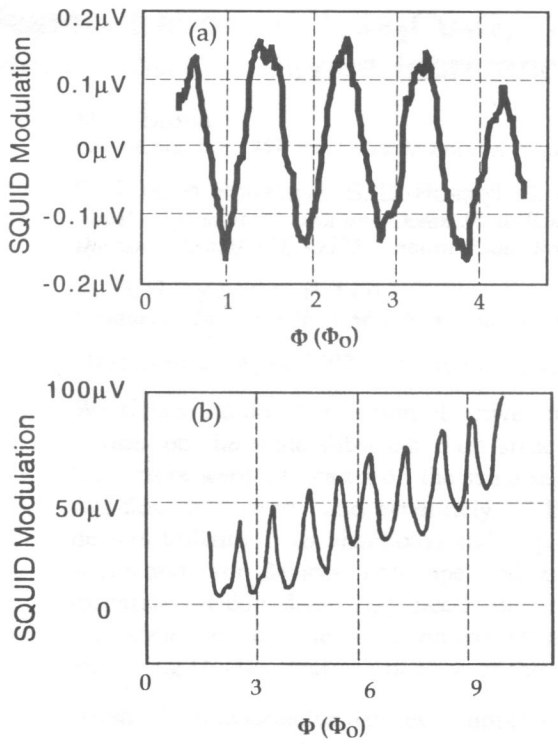

FIG. 2. (a) Modulation voltage at 77 K of one of the biepitaxial SQUIDs in Fig. 1. (b) Modulation voltage of a step edge SQUID at 77 K.

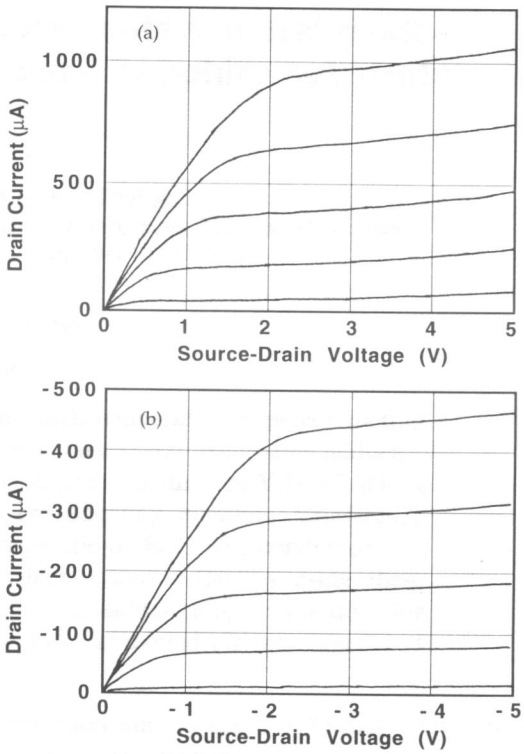

FIG. 4. *I-V* curves of two 3 μm$\times$20 μm (a) *n*-MOS and (b) *p*-MOS transistors at 300 K on the same sapphire wafer after cofabrication with the HTS biepitaxial SQUIDs. Source-drain voltages range from 0 to 5 V, at gate voltages from 1.0 to 3.0 V at 0.5 V increments.

gate width of 20 μm after the cofabrication of a working SQUID adjacent to it. The threshold voltage is measured to be about 0.8 V. In Fig. 4(b), the *I-V* curves of an identical size *p*MOS device is also shown after HTS fabrication. No significant difference was observed from characteristics measured prior to HTS fabrication. Both devices were also shown to function at 77 K.

In summary, we have performed the first fabrication of active semiconductor and high-temperature superconducting devices on the same substrate. Test structures of CMOS transistors were fabricated on the same sapphire substrate as test structures of YBCO flux-flow transistors, and separately, YBCO superconducting quantum interference devices exploiting step edge and biepitaxial Josephson junctions. Both semiconductor and superconductor devices were operated at 77 K. This cofabrication of these test structures on the same substrate opens the door for the fabrication of true semi/superconducting hybrid integrated circuits capable of exploiting the best of each of these technologies.

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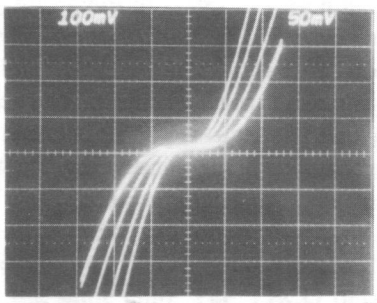

FIG. 3. The *I-V* curve of superconducting flux-flow transistor at various control line currents at 77 K.

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