Multichip module using multilayer $YBa_2Cu_3O_{7-\delta}$ interconnects

M. J. Burns, K. Char, B. F. Cole, W. S. Ruby, and S. A. Sachtjen
Conductus, Inc., 969 West Maude Avenue, Sunnyvale, California 94086

(Received 30 November 1992; accepted for publication 21 January 1993)

We report the first use of high temperature superconductors for multilayer interconnection of bare semiconductor die to form multichip modules. Ten die with a total of 160 pads were interconnected on a 3.4 cm^2 substrate. The interconnections were a combination of $YBa_2Cu_3O_{7-\delta}$ lines and vias on two wiring levels separated by an epitaxial insulating layer. Connection between the two $YBa_2Cu_3O_{7-\delta}$ wiring layers was accomplished by the use of superconducting vias through the insulator. Two similar multilayer multichip module designs, with 30- and 10-μm-wide $YBa_2Cu_3O_{\delta-7}$ lines, were constructed.

The need for high-performance alternatives to printed circuit (PC) boards has lead to the development of multichip modules (MCMs). MCMs use more compact unpackaged chips (die) spaced closely together, thus allowing a much higher areal density of function than PC boards can allow. A potential limitation on increases in functional density is that imposed by the resistivity of the interconnects. Conventional copper MCM interconnects are typically 100-μm wide and have been demonstrated down to the 20 μm range.[1] As linewidths decrease, higher functionality can be achieved, but at the expense of increasing line resistance. In high-speed circuits where the interconnects are impedance matched for 50Ω, signal lines typically must carry currents of 50–100 mA. Increased line resistance not only causes unwanted power dissipation, but also causes signal dispersion and increased cross talk.

For applications using complementary-metal-oxide-semiconductor (CMOS) or GaAs circuits whose performance can be enhanced by cooling to liquid nitrogen temperatures, another option is the use of high-T_c superconducting (HTS) materials for the interconnects. As high T_c materials such as $YBa_2Cu_3O_{7-\delta}$ (YBCO) remain superconducting at 77 K carrying currents up to typically $1–5\times10^6$ A/cm^2 (10–50 mA/μm^2) at 77 K, present HTS materials have the potential to allow the operation of MCM linewidths down to 1–2 μm and 3–6 μm pitches. Such small linewidths would enable a reduction of the number of interconnect layers needed in the MCM,[2] which should increase the ease of manufacturing a MCM for a given level of functionality. In order to provide a useful interconnect architecture, a HTS MCM must be of multilayer construction with a power plane, ground plane, and at least two wiring layers. To date, the most ambitious HTS multilayer device is a 3 HTS layer integrated superconducting quantum interference device (SQUID) magnetometer fabricated on a 1 cm^2 substrate.[3]

In this letter we describe a 10 CMOS chip, 3.4 cm square MCM constructed using a YBCO-insulator-YBCO multilayer configuration complete with vias for YBCO-YBCO connections through the insulator.

In Fig. 1 we show a photograph of a multilayer MCM with its wire-bonded bare CMOS die. The 9 inverter die[4] clustered in the 1 cm^2 area in the upper right of the module form a 5 MHz ring oscillator. The chip in the lower left of the module is a 12-bit binary counter die[5] which is configured to count the oscillations of the ring. The 12 pads along the bottom edge of the module are for the 12-bit output of the binary counter. The pads along the left edge of the module are for power connections and to allow cascading of multiple demonstration modules. YBCO lines were also routed throughout the module to allow all unused I/O pads on the die to be tied to the ground or supply potential, as appropriate. It should be noted that this specific MCM was designed to explore the limits of present-day large area HTS multilayer technology as applied to MCMs, rather than to perform a particularly useful function.

HTS multilayer deposition technology is presently most advanced for pulsed laser deposition; we have experience with over 20 HTS-compatible materials in our laboratory. However, uniform large-area coverage requires a specially designed laser deposition system.[6] On the other hand, multilayer capability for off-axis sputtering is currently limited to a few materials. However, it can more easily provide uniform coverage over 5 cm wafers.[7] For these reasons, we explored the fabrication of the HTS-insulator multilayer portions of these MCMs using a combination of both pulsed laser deposition and off-axis sputtering.

We used wafers of 1-mm-thick, 2-in.-diam $LaAlO_3$ as substrates. The architecture of the MCM was such that there was a main wiring layer composed of YBCO. In places requiring the crossing of wires, we made connections using vias through an insulating layer to YBCO lines on a first layer which crossed under the main (second) wiring layer. We laser deposited this 250–300-nm-thick YBCO film for the crossunders onto the substrate using standard deposition techniques.[3] The 40-μm-wide cross unders were patterned using conventional photolithographic techniques with AZ 4620 photoresist, Ar ion milling, and acetone resist stripping.

We then laser deposited the insulating layer, consisting of 500-nm-thick $SrTiO_3$, over the patterned crossunders. After masking with photoresist to define 40 μm square vias, the wafers were ion milled at an incident angle of 60° in a manner similar to that used for our SQUID processing.[3] The ion milling process continues until the vias break through all the way to the substrate. In Fig. 2 we show a schematic cross section of a completed via and in Fig. 3 we

 0003-6951/93/121435-03$06.00

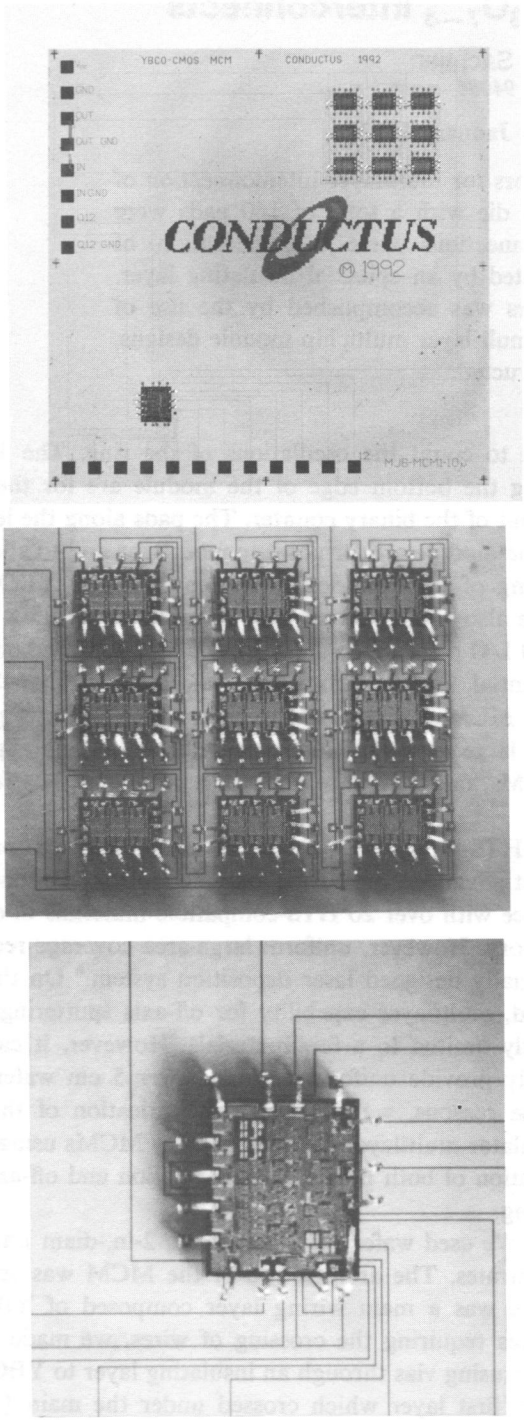

FIG. 1. HTS multilayer MCM using YBCO lines. (a) Completed multilayer module. The maximum line length is 7.5 cm. (b) Close-up of 9 chip CMOS ring oscillator interconnected with YBCO. (c) Close-up of CMOS binary counter chip. Note that many YBCO interconnects pass under this chip.

show a successive series of close-up photographs of one such via, along with a nearby crossunder.

After the vias have been opened, we then grow a third layer composed of approximately 250 nm of YBCO. In the case of the 30 μm linewidth MCMs, this YBCO layer was grown in two stages. First, approximately 30 nm of YBCO is deposited by laser deposition. Then the wafer is transferred into an off-axis sputtering system while still mounted on its substrate holder. The remaining 250 nm of

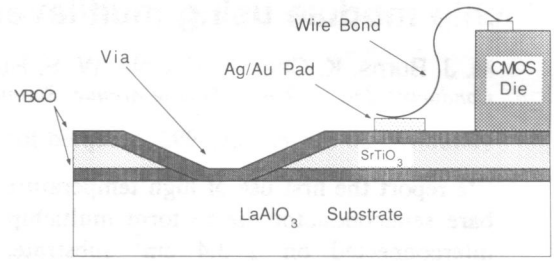

FIG. 2. Schematic cross section of a HTS crossunder and vias. Epitaxy is maintained from the substrate through the top YBCO layer.

YBCO is deposited by off-axis sputtering. In the case of the 10 μm linewidth MCM, we grew this YBCO layer by scanning laser deposition in which the substrate is moved through the laser plume to cover the whole 2-in-diam wafer.[6] We then patterned this final YBCO layer using standard photolithography and Ar ion milling to form the main wiring layer.

Finally, we define the fourth layer for the MCM contact and wire-bonding pads using a liftoff process with Ar ion beam cleaning *in situ* followed by 150 nm of Ag followed by 150 nm of Au. These Ag/Au contacts provide low-resistance contacts to the YBCO while also providing a chemically inert surface for subsequent wire bonding.

We attached the CMOS die using GE-7031 varnish, a standard cryogenic bonding agent.[8] Prior tests of CMOS die bonded using this bonding agent over a bare 20 μm YBCO line established that there was no degradation of the underlying YBCO with repeated cycling between 300 and 77 K.

The 10 CMOS die were electrically connected to the Ag/Au YBCO contact pads with 160 ultrasonic wire bonds. Both 0.003 in. $\times$0.0005 in. Al ribbon and 0.003 in. $\times$0.0005 in. Au ribbon were used successfully on different modules.

Verification of the YBCO and $SrTiO_3$ electronic properties were performed on the finished module at room temperature and at 77 K while the modules were immersed in liquid nitrogen. For example, in the measured YBCO line

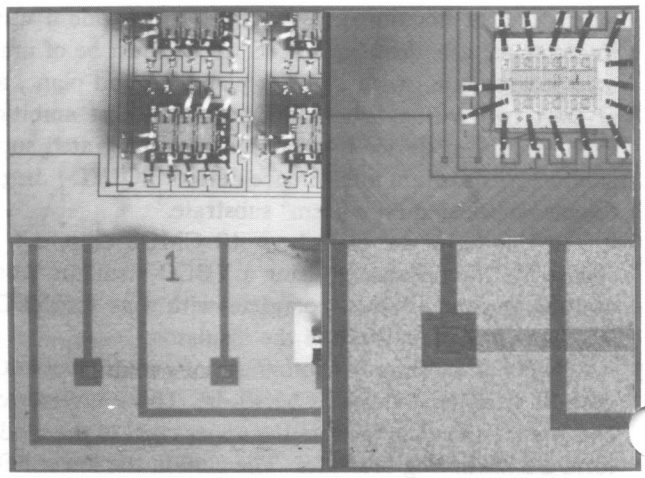

FIG. 3. View of one of the epitaxial vias under successive magnification.

resistivities were 240 $\mu\Omega$ cm at 300 K, dropping to 0 $\mu\Omega$ cm at the superconducting transition temperature of ~ 87 K. Currents up to 100 mA were passed through the lines at 77 K, which remained superconducting, indicating the line critical current density to be greater than 3×10^6 A/cm^2 at 77 K. Lines containing vias remained superconducting at 77 K for currents up to 15 mA, indicating a via critical current density of 3.1×10^4 A/cm^2 at 77 K. This reduced via critical current most likely is due to a combination of disorder and grain boundaries at the via YBCO-YBCO interface. The 0.5-μm-thick $SrTiO_3$ insulating layer used to isolate crossing lines displayed a measured resistivity of 4.8×10^3 Ω cm at 300 K, rising to 2×10^6 Ω cm at 77 K.

In Fig. 4 we show the output of the ring oscillator on the 30 μm MCM as well as the first bit ($\div 2$ output) and twelfth bit ($\div 2^{12}$ output) at 77 K. Testing of the modules was performed in a liquid nitrogen cooled test jig fitted with pogo pins for contacting the MCM I/O and power pads. The modules were first powered up while at room temperature. Because of the high normal state resistance of the YBCO (200–300 $\mu\Omega$ cm), the modules would not operate at 300 K. Power was removed from the modules and they were immersed in liquid nitrogen (77 K). To minimize moisture condensation, the jig was cooled and operated in a dry N_2 gas environment. Once the modules were cooled to 77 K, the power was reapplied. The modules operated successfully over a supply range of 3 to 15 V.

In the future, for HTS technology to offer a viable MCM interconnect option for cooled CMOS/GaAs, it will require a considerable extension of the work presented in this letter. A HTS MCM will require a HTS power plane separated from a HTS ground plane by about 0.1 μm of insulator to form a distributed capacitor, a 1–2-μm-thick insulator with a low (ideally <5) dielectric constant, two HTS wiring layers composed of 1–3 μm lines, and small area vias between all of the layers. Some of the materials used for this demonstration, particularly the $SrTiO_3$ dielectric and the $LaAlO_3$ substrate, will not be appropriate for technologically useful MCMs. The entire MCM structure will have to be fabricated so as to maintain the epitaxial quality of all four HTS layers over perhaps a 100 cm^2 area, and must maintain high critical current densities for all lines and vias. An in-process repair strategy will also need to be developed, probably an epitaxial one. At present such a structure probably could not be built using *any* known technology. To build it with HTS will certainly represent a challenge for the HTS community, but one that if met will have substantial benefits for advanced electronic systems.

In conclusion, we have demonstrated the world's first fully functional multilayer high temperature superconductor multichip modules. These demonstration units incorporated large area (3.4 cm$\times$3.4 cm) multilayer YBCO, two levels of interconnects as long as 7.5 cm, superconducting vias between levels and 10 CMOS die with 160 CMOS-MCM wire bonds. The lines displayed critical current densities over 3×10^6 A/cm^2 (30 mA/μm^2) sufficient for most anticipated applications. Two versions were fabricated, using 10 and 30 μm YBCO linewidths, of which the 30 μm version operated without the need for repairs to broken lines. We have thus demonstrated many of the key elements needed in multichip modules. The modules were fully tested and found to be fully functional at 77 K.

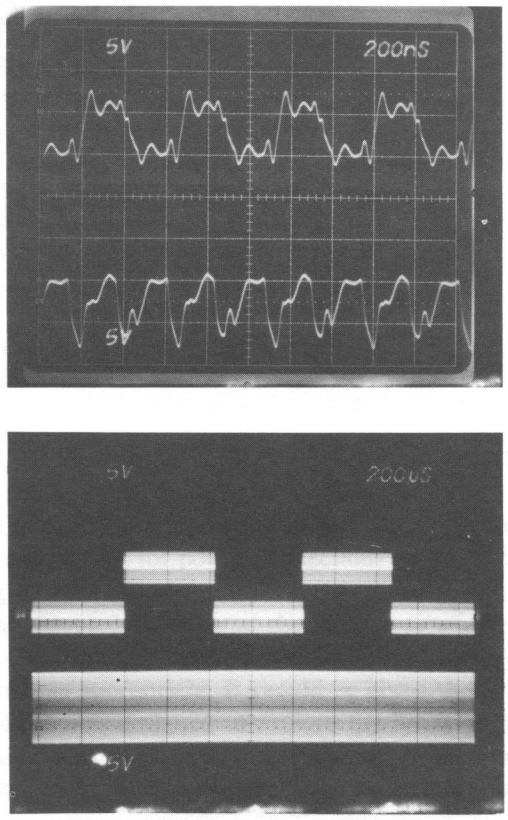

FIG. 4. (a) 2.5 MHz scope trace of bit 1 ($\div 2$) of the 12-bit counter (top) and the 5 MHz ring oscillator (bottom). (b) 1.2 kHz scope trace of bit 12 ($\div 2^{12}$) of the 12-bit counter (top) and the 5 MHz ring oscillator (bottom).

We would like to acknowledge valuable technical discussions with Richard Eden, Paul Kohl, Boo Nilsson, Lincoln Bourne, John Rowell, Randy Simon, and Stuart Wolf. This work supported by the DARPA HTS MCM program.

[1] See, for example, J. M. Segelken, L. J. Wu, M. Y. Lau, K. L. Tai, R. R. Shively, and T. G. Grau, IEEE Trans. Comp. Hybrids, Manuf. Technol. **15**, 438 (1992).

[2] For example, R. R. Tummala and S. Ahmed, IEEE Trans. Comp. Hybrids, Manuf. Technol. **15**, 426 (1992). The authors describe the need for 65 interconnect layers in the IBM ES/9000 MCM, 63 thick film layers which use 75 μm linewidths, 450 μm pitch, and 2 thin film layers which use 25 μm linewidths, 55 μm pitch.

[3] L. P. Lee, K. Char, M. S. Colclough, and G. Zaharchuk, Appl. Phys. Lett. **59**, 3051 (1991).

[4] CD4009UBH type Hex Buffer (Inverting), manufactured by RCA Solid State Division.

[5] CD4040BH type 12-Stage Ripple Carry Binary Counter, manufactured by RCA Solid State Division.

[6] S. R. Foltyn, R. E. Muenchausen, R. C. Dye, X. D. Wu, L. Luo, D. W. Cooke, and R. C. Taber, Appl. Phys. Lett. **59**, 1374 (1991); also see, for example, J. A. Greer, J. Vac. Sci. Technol. A **10**, 1821 (1992).

[7] W. Y. Lee, J. Salem, V. Lee, T. Huang, R. Savoy, V. Deline, and J. Duran, Appl. Phys. Lett. **52**, 2263 (1988); also see, for example, N. Newman, B. F. Cole, S. M. Garrison, K. Char, and R. C. Taber, IEEE Trans. Magn. **MAG-27**, 1276 (1991).

[8] GE-7031 varnish manufactured by the General Electric Corp., Schenectady, New York.