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Demonstration of Sapphire as a Common Substrate for Monolithic Co-fabrication of $Y_1Ba_2Cu_3O_{7-\delta}$ and SOS CMOS Devices

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In the seven years since the discovery of high-temperature superconductors (HTS), the field of superconductive electronics has undergone explosive development. Due to difficulties in growing films directly on silicon, copper and oxygen contamination of the silicon layers during growth, and the high temperature environments seen in HTS growth, it has not been fully integrated with semiconductor based technology. Research has been focused on the use of superconducting interconnects between integrated circuits, which could lower chip power dissipation, reduce necessary interconnect width and pitch, and reduce dispersive loss. Several attempts have been made to fabricate HTS circuits or devices directly on Si or other semiconductor surfaces[1,2]; these layers were of low quality and were stress limited, and no devices were fabricated in the layers.

The 1102 sapphire plane usually used for SOS fabrication is, however, one of the preferred substrates for growth of the YBCO layers necessary for HTS devices. In addition, the sapphire acts as a good diffusion barrier, and for low temperature operation, the increased CMOS SOS p-channel mobility gives the combination an additional advantage over other silicon technologies[3].

Figure 1 shows a schematic cross sectional view of monolithically co-fabricated HTS and CMOS devices on the same sapphire substrate. Fabrication of the thin-film SOS CMOS was performed first as described elsewhere[4]. Areas that were to later have HTS devices were initially protected from various silicon processing steps such as high energy ion implants by not removing the silicon layer from the area. As the aluminum interconnect layer could not withstand the processing temperatures incumbent in superconducting device fabrication, over short distances it was replaced by a second polycide ($TiSi_2$) layer. After CMOS processing was complete, the silicon protective coating was removed in the HTS area and a 200 nm layer of Si_3N_4 was deposited and patterned over the CMOS devices as a final passivating layer against the oxygen plasma and copper environments seen during the YBCO growth.

YBCO bi-epitaxial and step edge superconducting quantum interference devices (SQUIDs) and flux-flow transistors (FFTs) were then fabricated on the bare sapphire adjacent to the test CMOS devices, aligned lithographically. Pulsed laser deposition (PLD) techniques were used[5] in conjunction with a series of buffer layers[6]. For the production of grain-boundary SQUIDs, these buffer layers include final MgO and CeO layers used to produce a 45° in-plane rotation where desired. An amorphous Al_2O_3 layer was used as a passivation of the YBCO devices. Openings for electrical contact to both the YBCO devices and the CMOS can be made using photolithography and RIE or ion milling and a final layer of metal can easily be patterned for a final interconnection layer.

All devices functioned as expected at 77 K without degradation, demonstrating that a compatible process has been found to monolithically integrate adjacent CMOS and HTS devices. Figure 2 shows the I-V curves from a representative n-MOS device at 77 K after HTS device co-fabrication. Figure 3 shows a step-edge SQUID with a modulation voltage at 77 K of $40\mu V/\Phi_0$, also monolithically co-fabricated with SOS CMOS.

Numerous other possibilities to explore the combination of these two well developed technologies exist. Circuits and devices that exploit the advantages of both HTS materials and SOS CMOS in order to mitigate the deficiencies of the other can be integrated together. For example, ultra-sensitive SQUIDs, bolometers, and ultra-high speed FFTs and Josephson Junction based circuits (functioning at speeds of 100 GHz or more) can be combined with CMOS memories, latches, low noise amplifiers, silicon based sensors, and driving electronics.

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[1] D.K. Fork, D.B. Fenner, R.W. Barton, J.M. Philips, G.A.N. Connell, J.B. Boyce, T.H. Geballe. *Appl. Phys. Lett.*, 57, 1161, 1990.
[2] D.K. Fork, K. Nashimoto, T.H. Geballe. *Appl. Phys. Lett.*, 60, 1621, 1991.
[3] M. Roser, S.R. Clayton, P.R. de la Houssaye, G.A. Garcia. Presented at 50th DRC, 1992.
[4] B.W. Offord. 4th NASA Symposium on VLSI Design 1992, University of Idaho, October 29-30, 1992.
[5] K. Char, M.S. Colclough, S.M. Garrison, N. Newman and G. Zaharchuk. *Appl. Phys. Lett.* 59, 733 (1991).
[6] L.P. Lee, K. Char, M.S. Colclough, and G. Zaharchuk. *Appl. Phys. Lett.* 59, 3051 (1991).

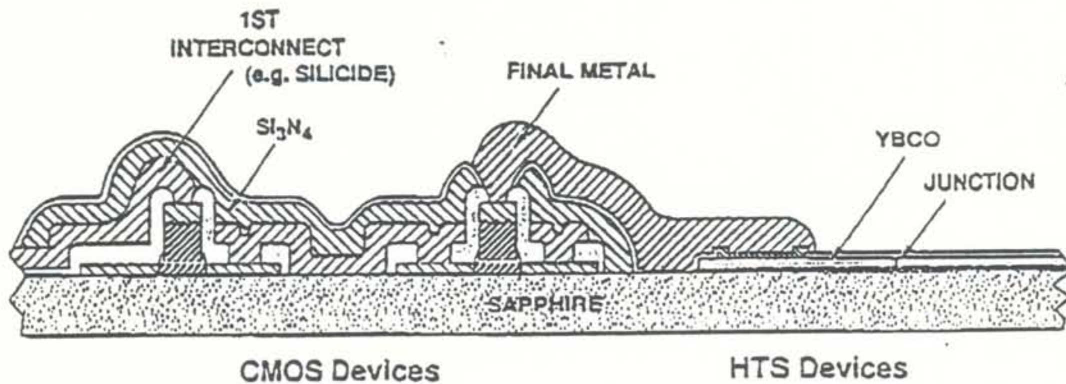

Figure 1. Cross-sectional Shematic View of Monolithically Co-fabricated CMOS and HTS Devices

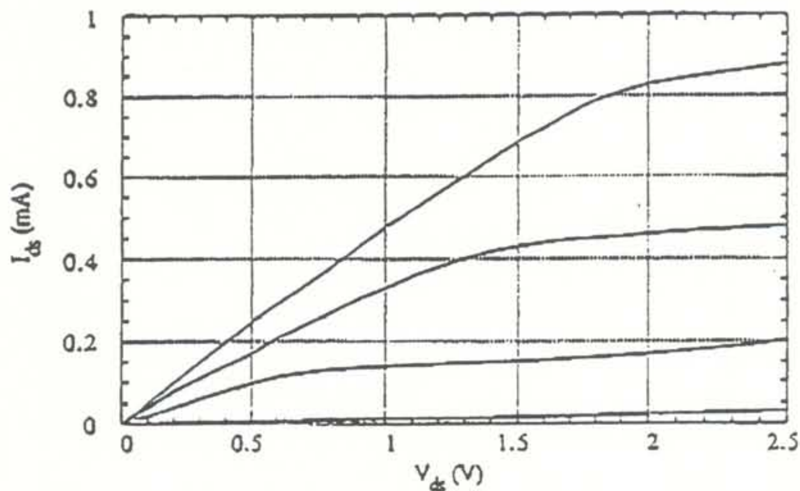

Figure 2. 6μm x 20μm NMOS Measured at 77K After Co-fabrication of HTS Devices. V_g steps are 0.5 Volts from 1.5 to 3.0 Volts

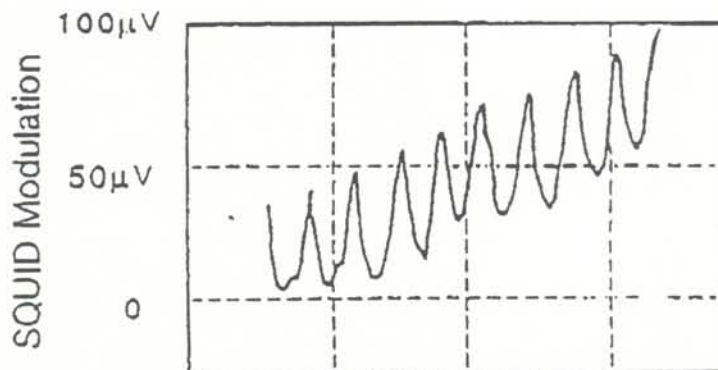

Figure 3. Functional Step-edge SQUID Monolithically Co-fabricated on CMOS/SOS