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DESIGN OF HETROEPITAXIAL MULTILAYER STRUCTURES FOR HIGH T_c SUPERCONDUCTOR INTEGRATED CIRCUITS.

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We are establishing a multi-level high T_c superconducting (HTS) microelectronics technology based on pulsed laser deposited or sputtered thin films. Integrated circuit structures of HTS materials need to be built from an entirely epitaxial technology, in which successive layers must be highly aligned in both the growth direction and in plane.

Ex situ patterning of thin film wires, via contacts between wires, epitaxial step coverage, and Josepson junctions are additional requirements for this technology. Nevertheless, pinhole free epitaxial insulators for large area (2" diameter chip area) applications are still a challenging problem on large substrates such as $LaAlO_3$ and yttria-stabilized zirconia(YSZ). Between a $YBa_2Cu_3O_7$ ground plane and wiring layers, $SrTiO_3$, CeO_2, $LaAlO_3$, Y_2O_3, YSZ, or $PrBa_2Cu_3O_7$ were used as insulators. Combinations of above thin insulator films were also developed as heteroepitaxial insulators. The effect of processing parameters on particulate density and surface morphology will be discussed. The critical control of the dry or wet etching profile of each layer will be discussed for step coverage that must be free of weak links. Our progress towards large area integrated circuit structures, e.g. a multichip module, with planarization techniques will be reported as well.

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